

FIG. 1
PRIOR ART

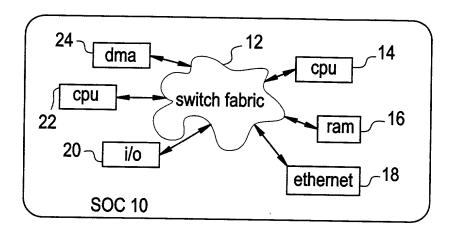


FIG. 2

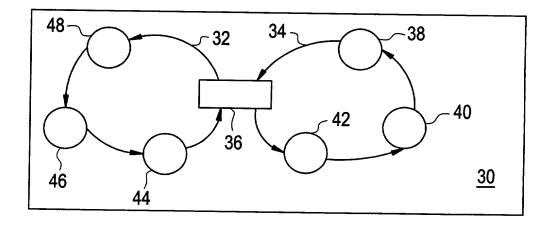




FIG. 3

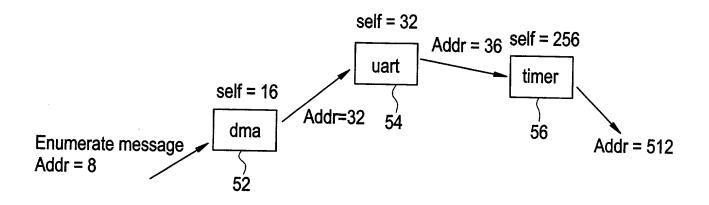


FIG. 4

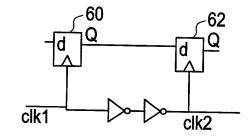


FIG. 5

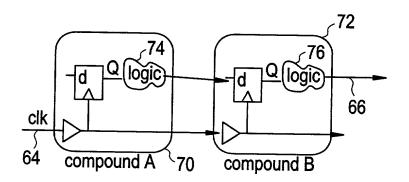




FIG. 6

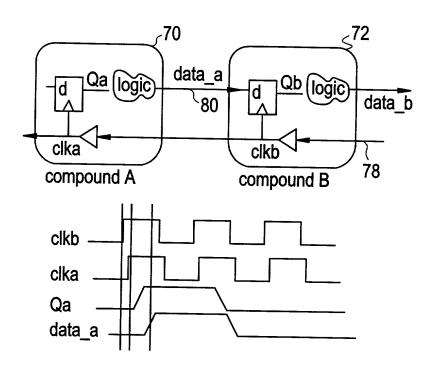


FIG. 7

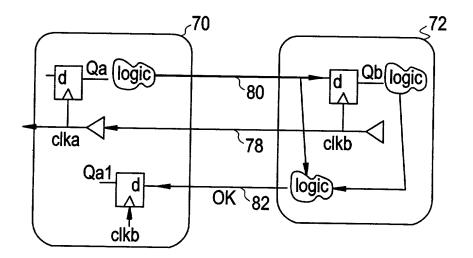




FIG. 8

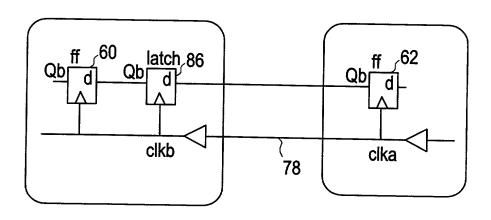


FIG. 9

clka
clkb
data_a

96
data_a

94
clock



FIG. 10

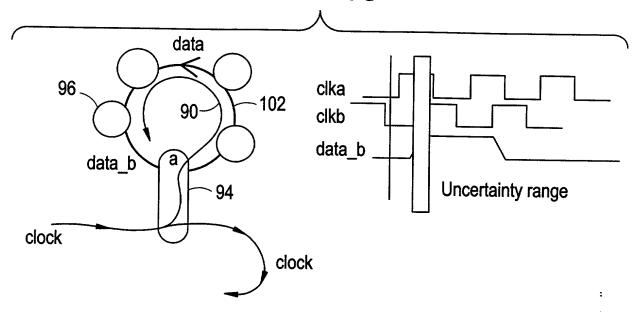


FIG. 11

local_clock 110

data_in local_data_out 116

data from previous member clk clock

FIG. 12

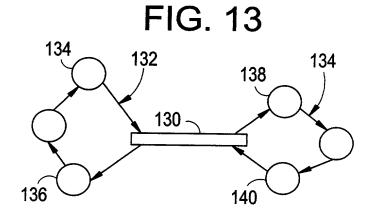




FIG. 14

150

158

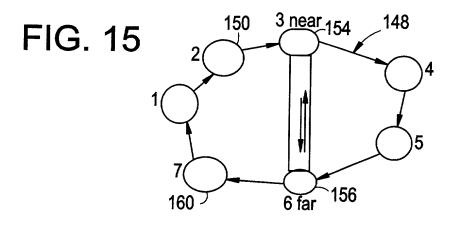
158

150

158

158

158



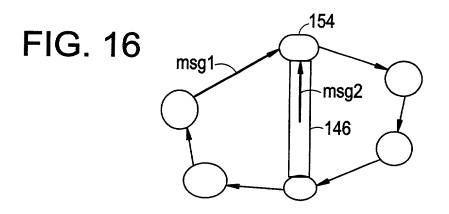




FIG. 17

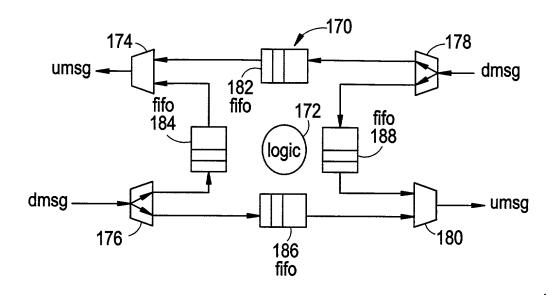
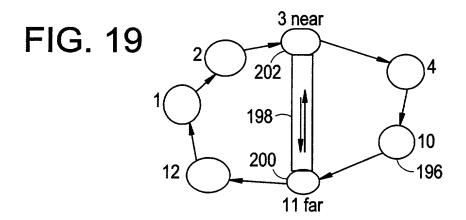


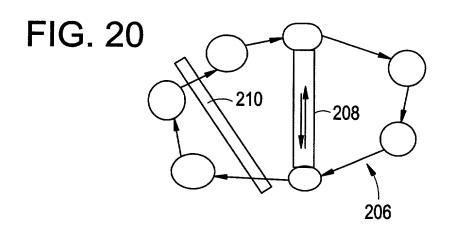
FIG. 18

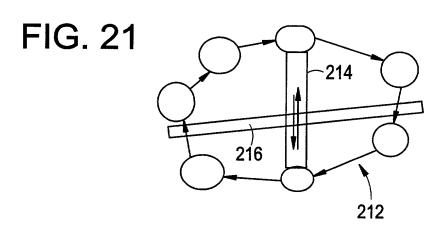
192

near far









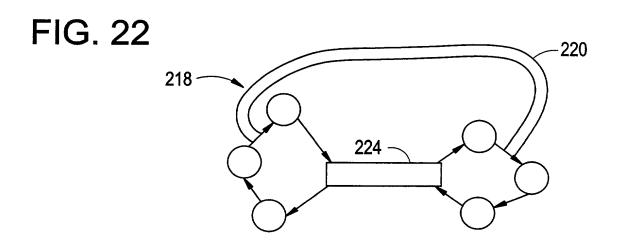




FIG. 23

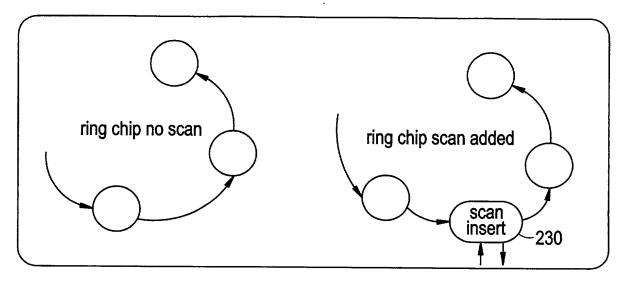


FIG. 24

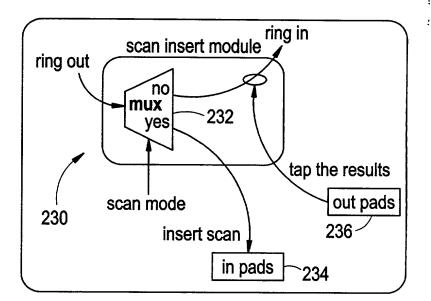


FIG. 25

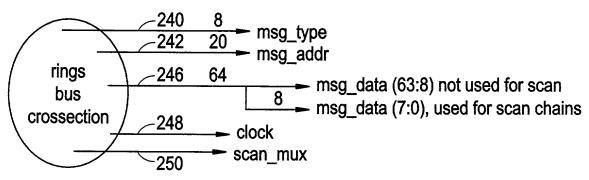




FIG. 26

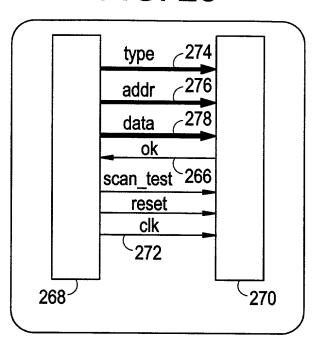


FIG. 27

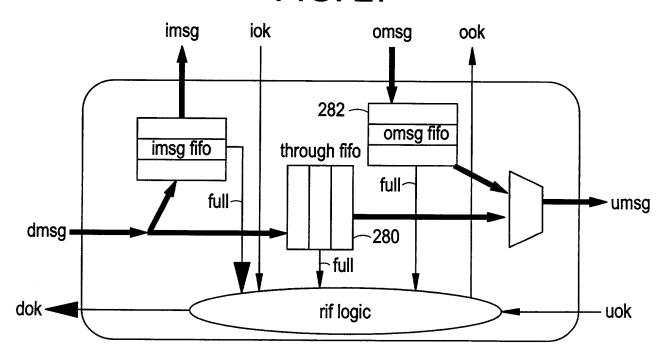




FIG. 29

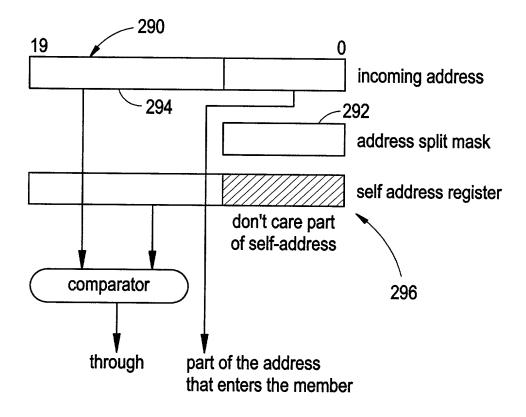




FIG. 30

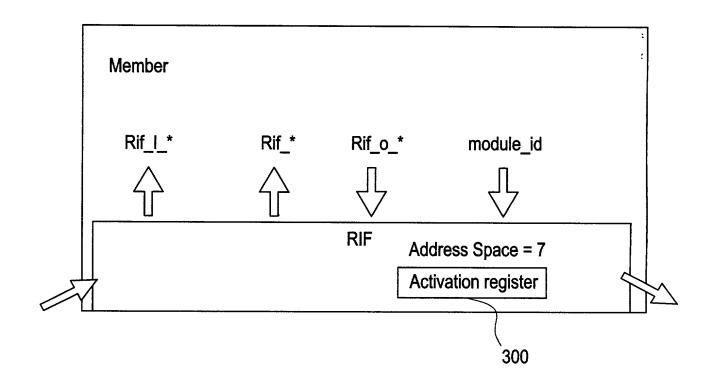




FIG. 31

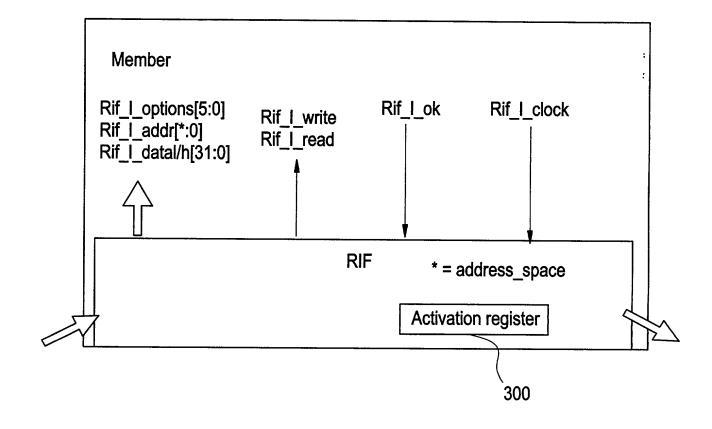




FIG. 32

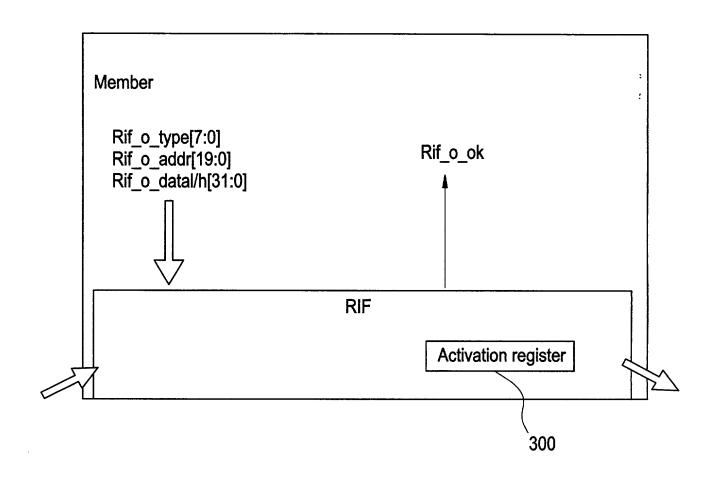
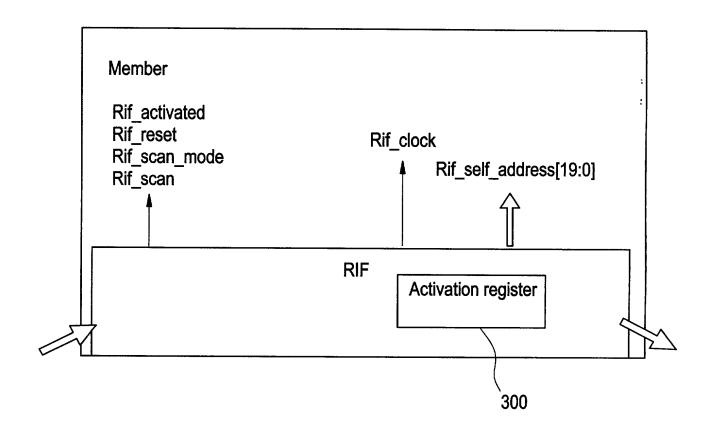




FIG. 33



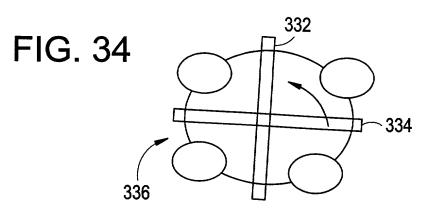
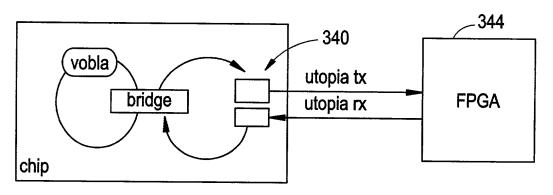
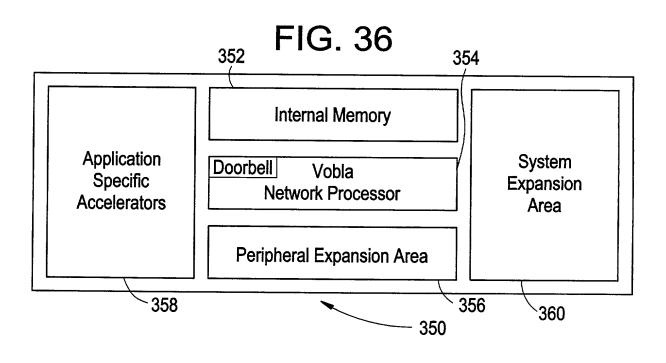
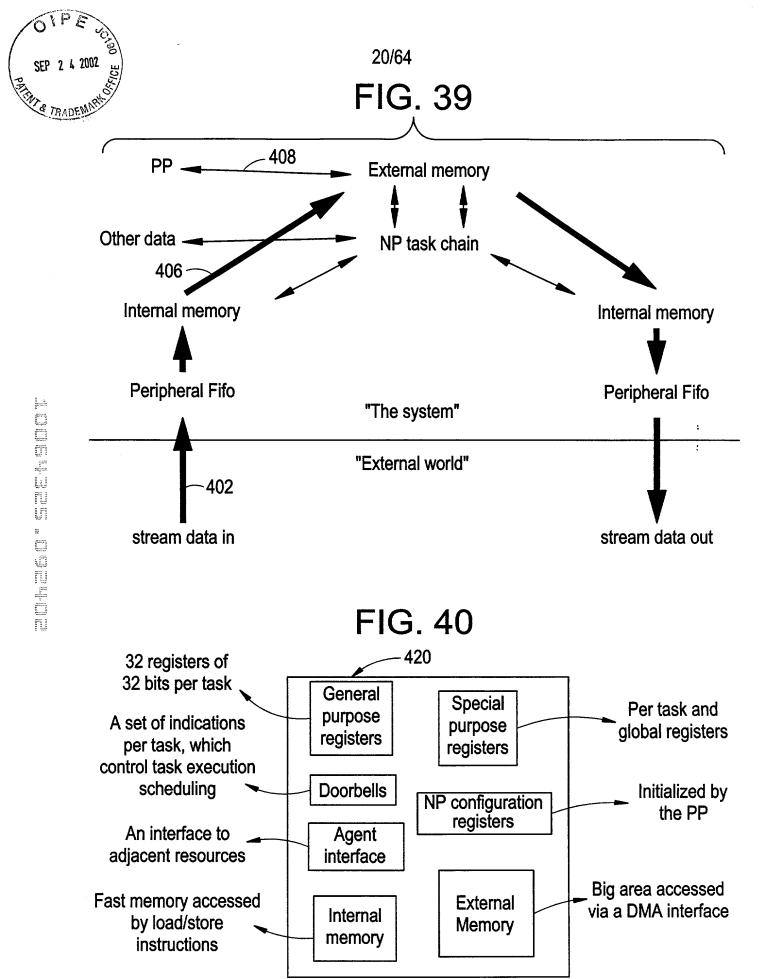


FIG. 35





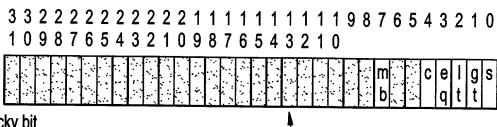




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FIG. 41

R1 register



430

446

s - sticky bit

eq - equal/zero

It - less then/negative

gt - greater then/positive

c - carry

(spr index - 3)

mb - reflection of the RAM mult-reader busy indication

FIG. 42

REFETCH SPR (spr index - 0)	NEXT_REFETCH	REFETCH 440				
TASK SPR D	3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5	1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0 5 4 3 2 1 0 NTID CTID				
(Spi ilidex - 1)	3 2 2 2 2 2 2 2 2 2 1 1 1 1 1	1 1 1 1 1 9 8 7 6 5 4 3 2 1 0				
TRAP SPR (spr index - 2)	0987654321098765	5 4 3 2 1 0 Y T D P T D B B A A R L B B A P 444				
	3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5	111119876543210 543210 INDEX1				





FIG. 43

		4	50		
	common task data			1	size of level0 frame part is
r27	task fragment 1 data	task fragment 2 data	task fragment 3 data		different for each task type
	data of all level2 functions			A	size of level2 frame part is constant
	level1 f1 data	level1 f2 data	level1 f3 data		size of level1 frame part is different per
					each task type

SEP 2 1 2002 SEP 2 1 RADEMARK

special purpose mux/ 460 daiu_in_mux, data alu data_wt2 data_rd2 align 8 용 2 align qps <u>==</u> rf_in_mux FIG. 44 address 2 addr alu mux register file dab internal memory <u>ب</u> 2 address 1 9 /mux pc2 vector refetch next decode logic FBIL data_rd1 2 controls g

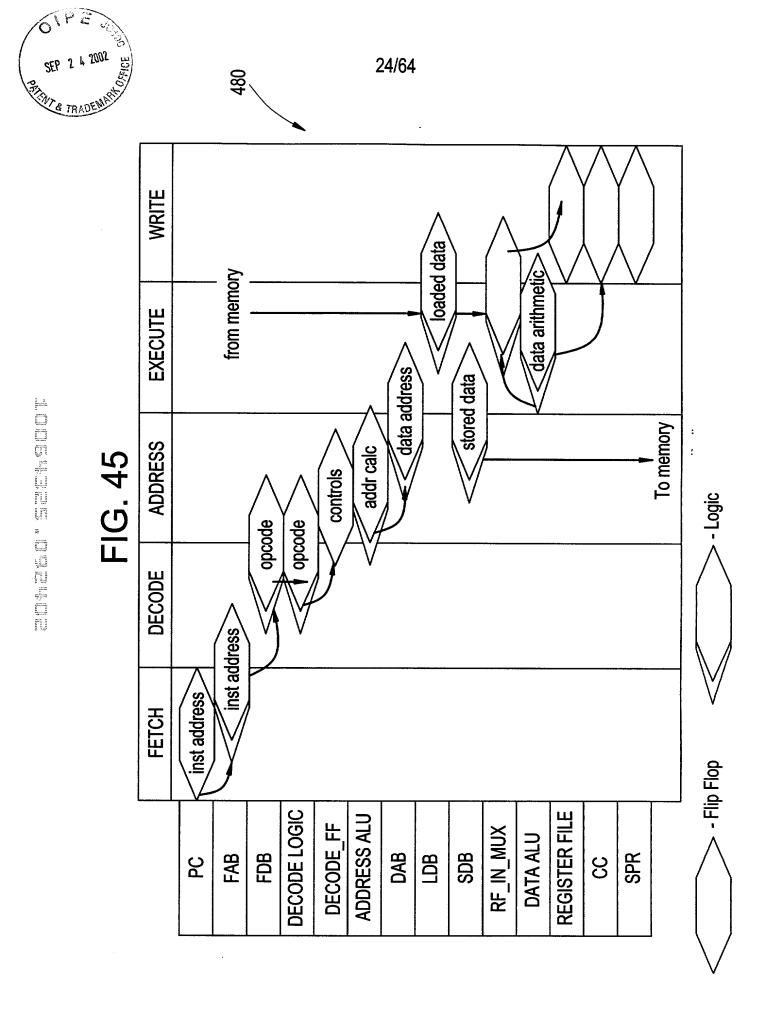




FIG. 46

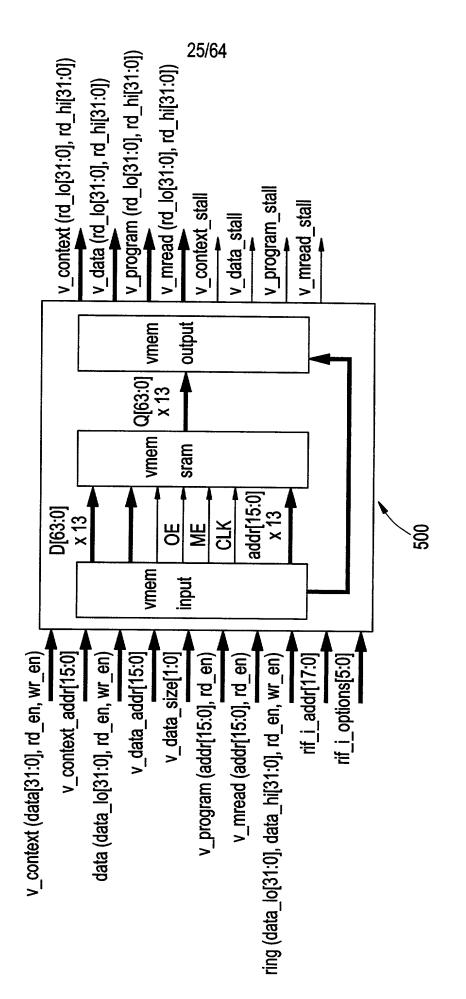
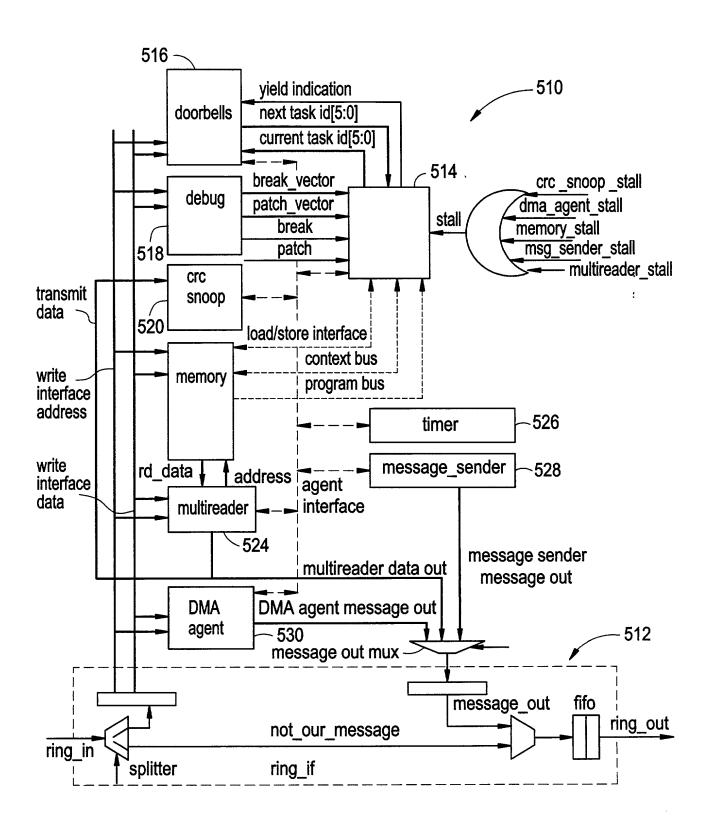
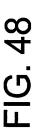


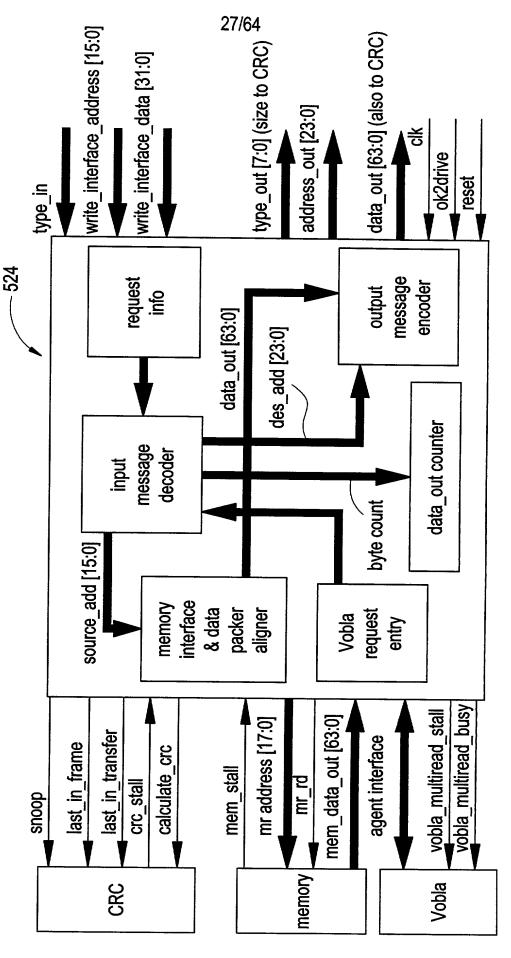


FIG. 47











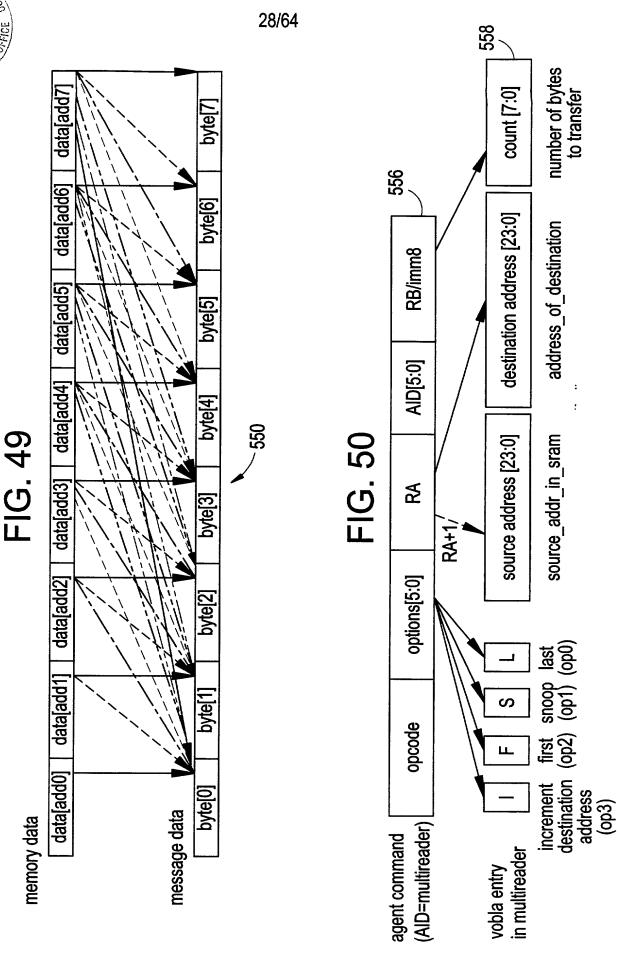
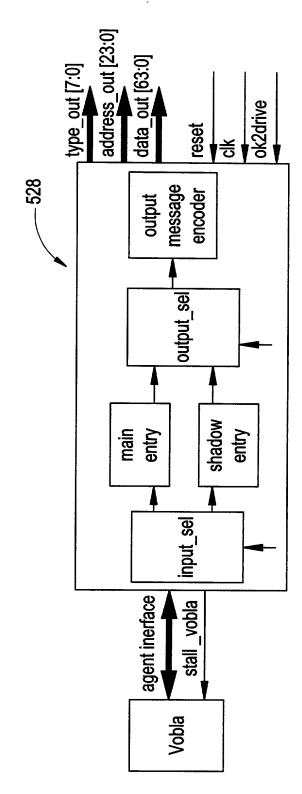




FIG. 51







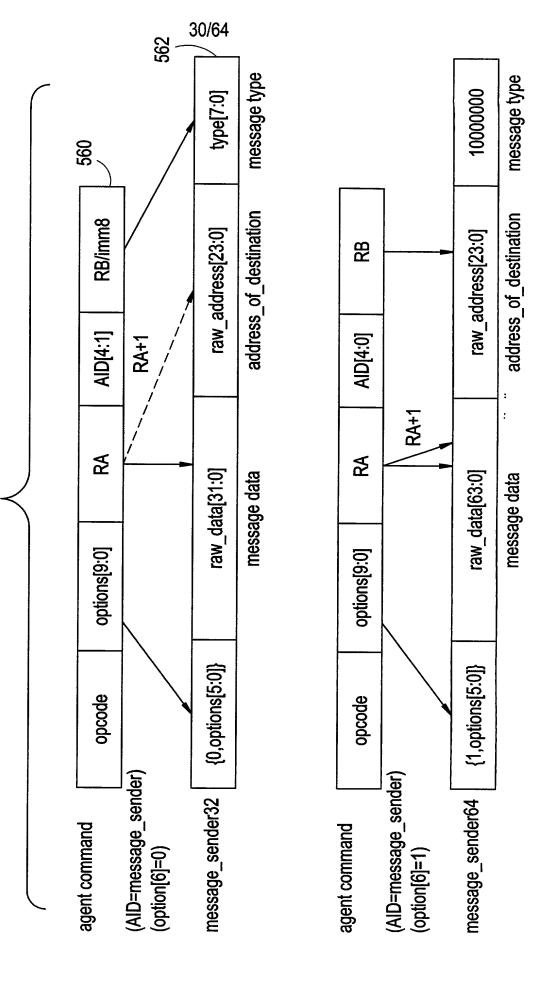




FIG. 53

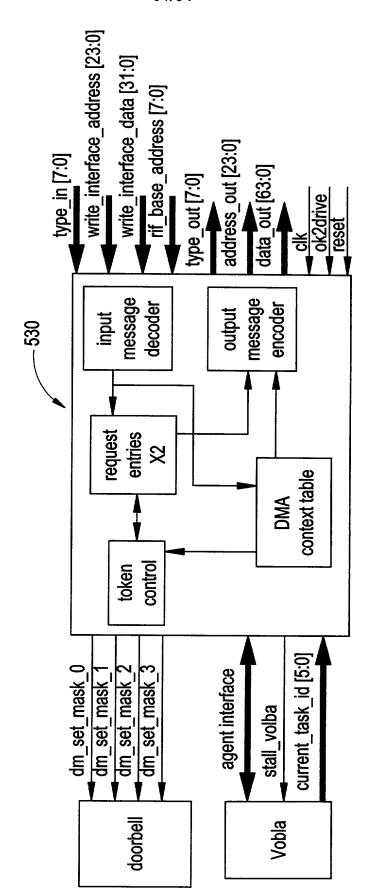




FIG. 54

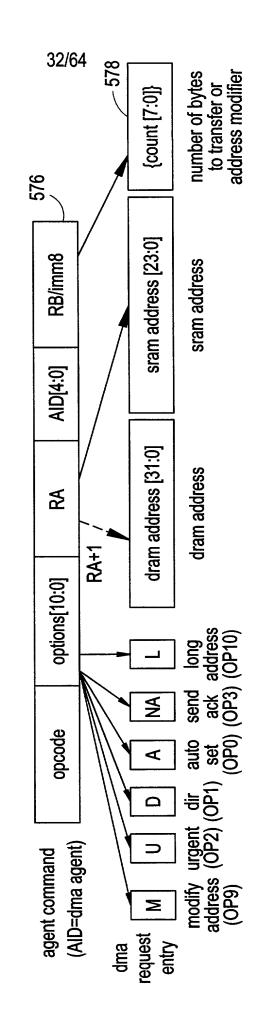




FIG. 55

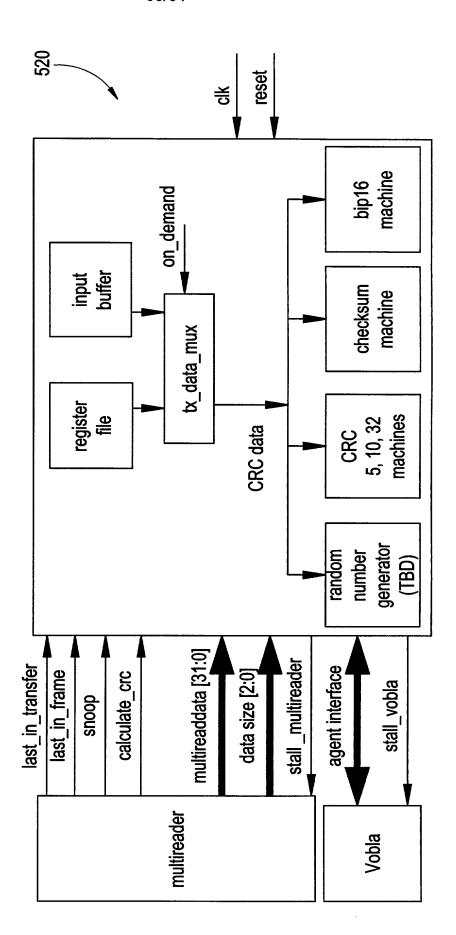




FIG. 56

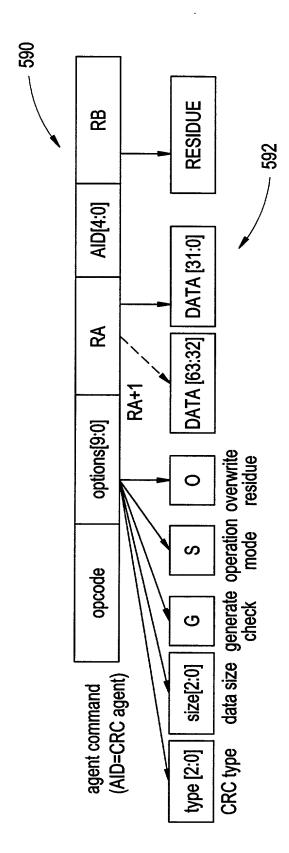




FIG. 57

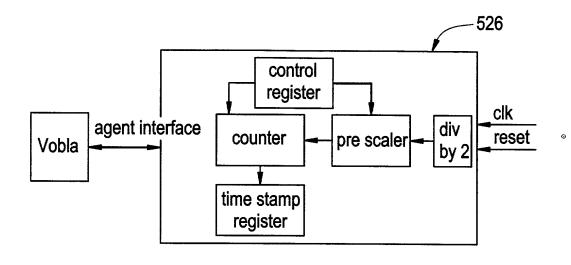
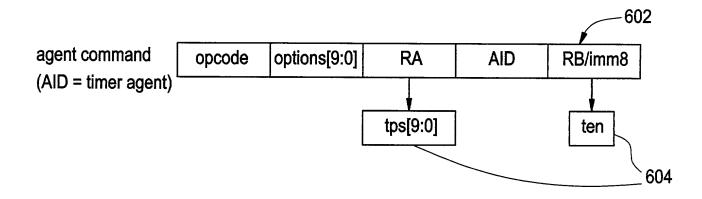


FIG. 58



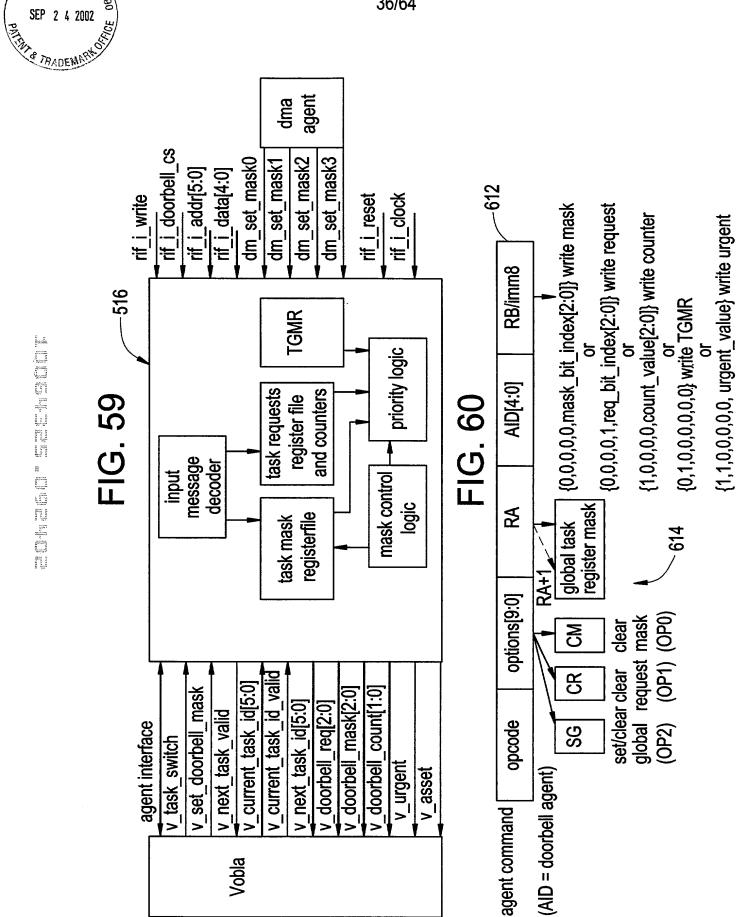
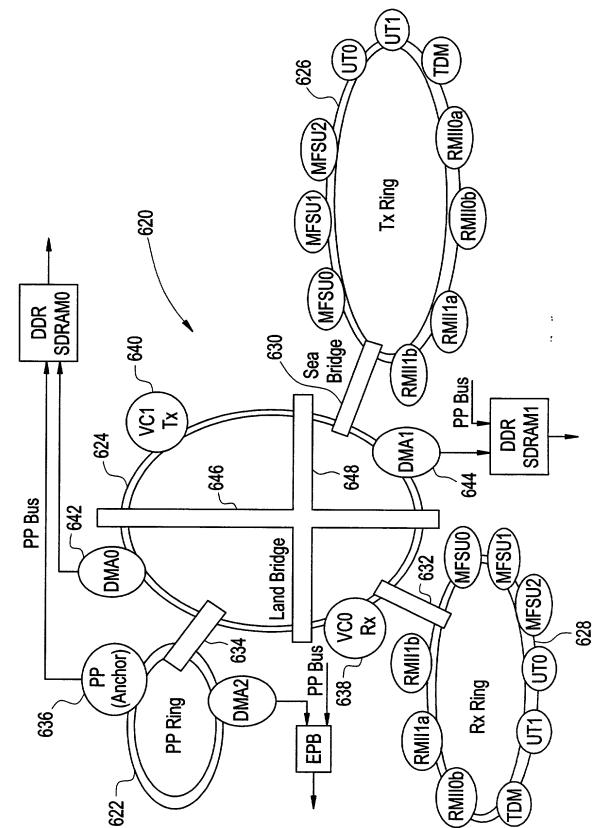
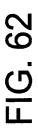




FIG. 61







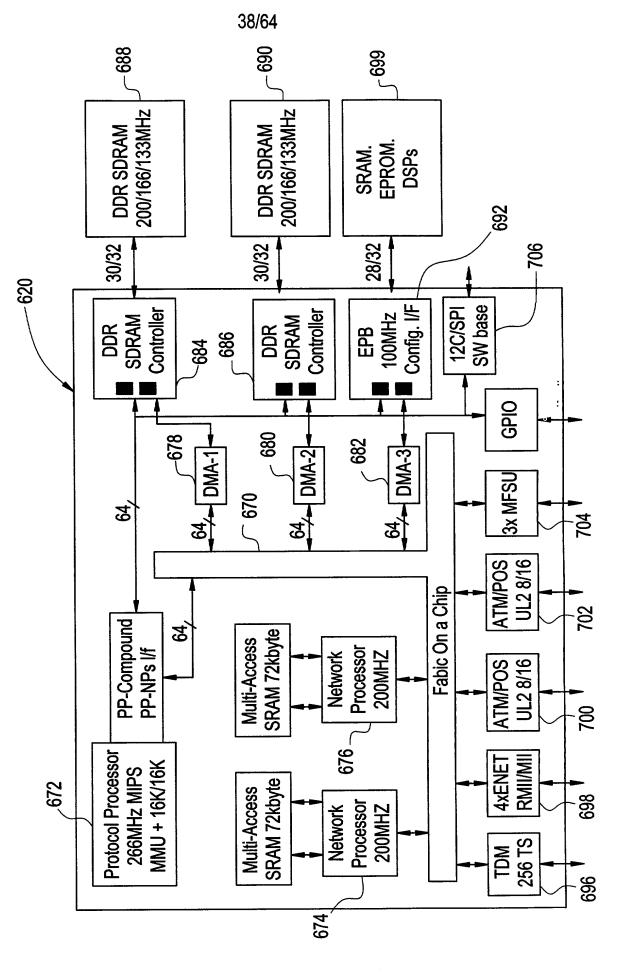




FIG. 63

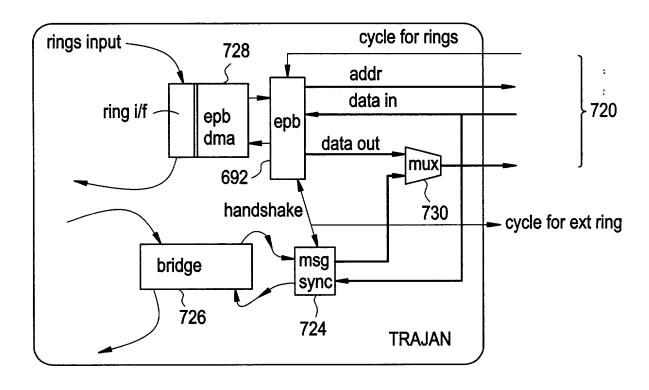
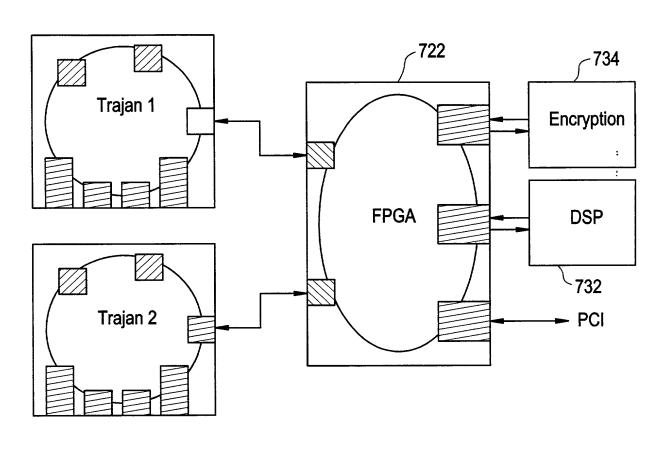




FIG. 64



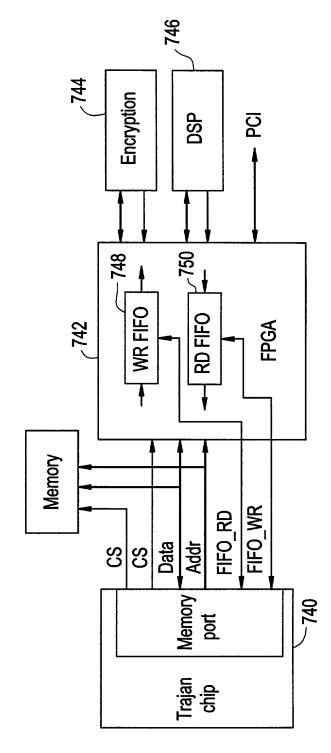
Processor

Functional unit

External ring interface



FIG. 65





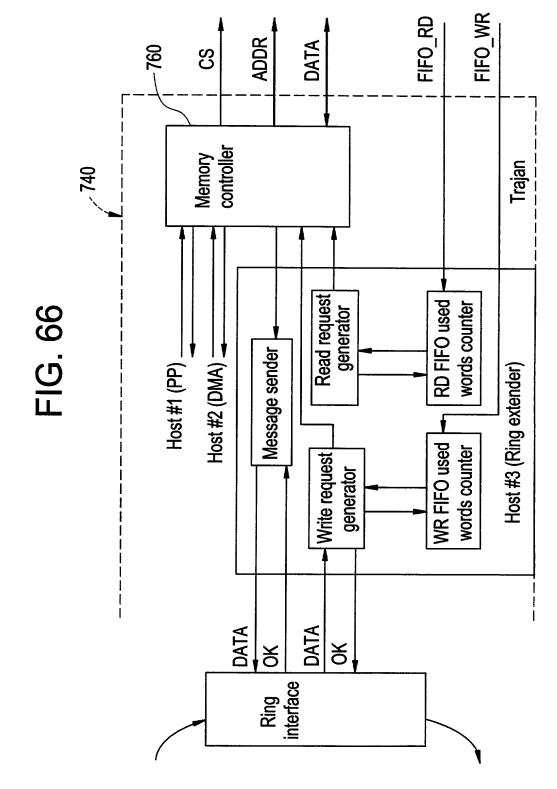




FIG. 67

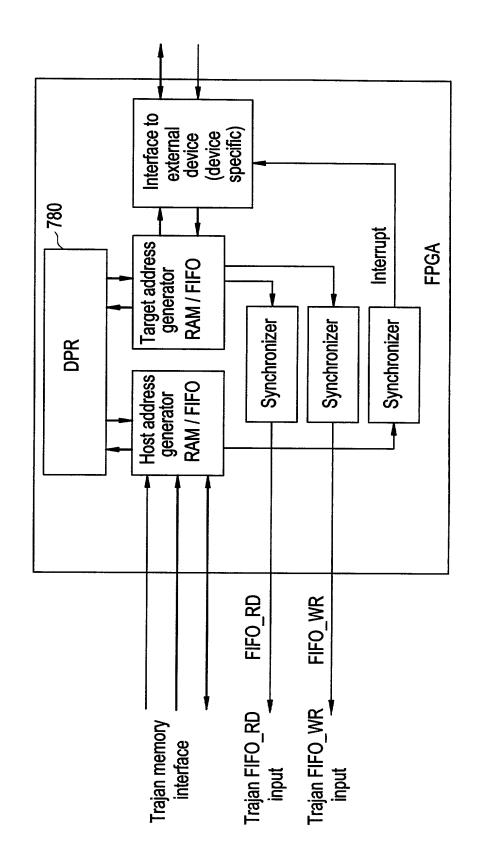




FIG. 68

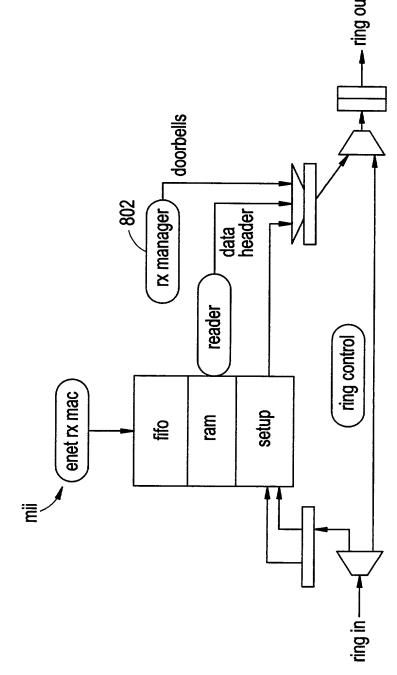
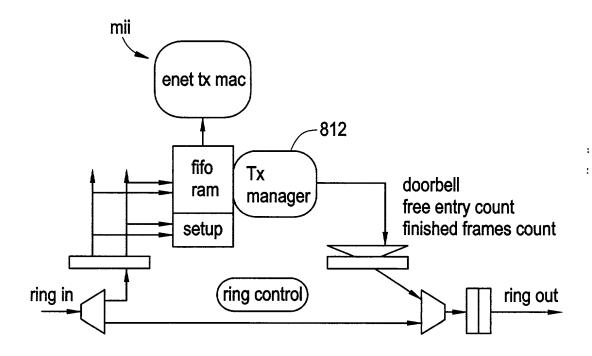
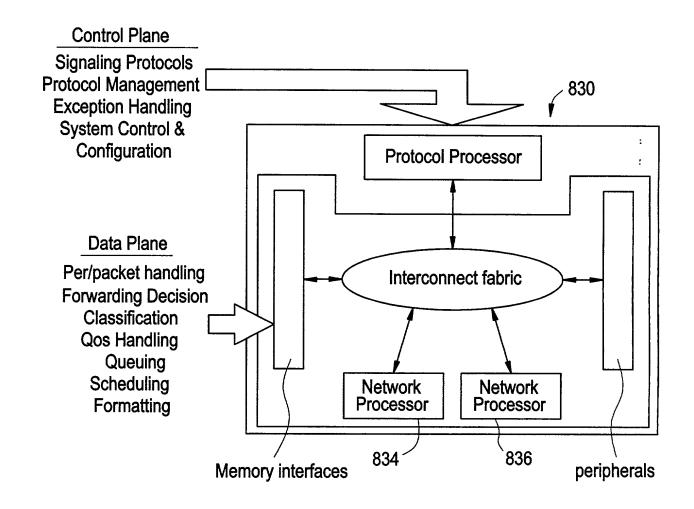


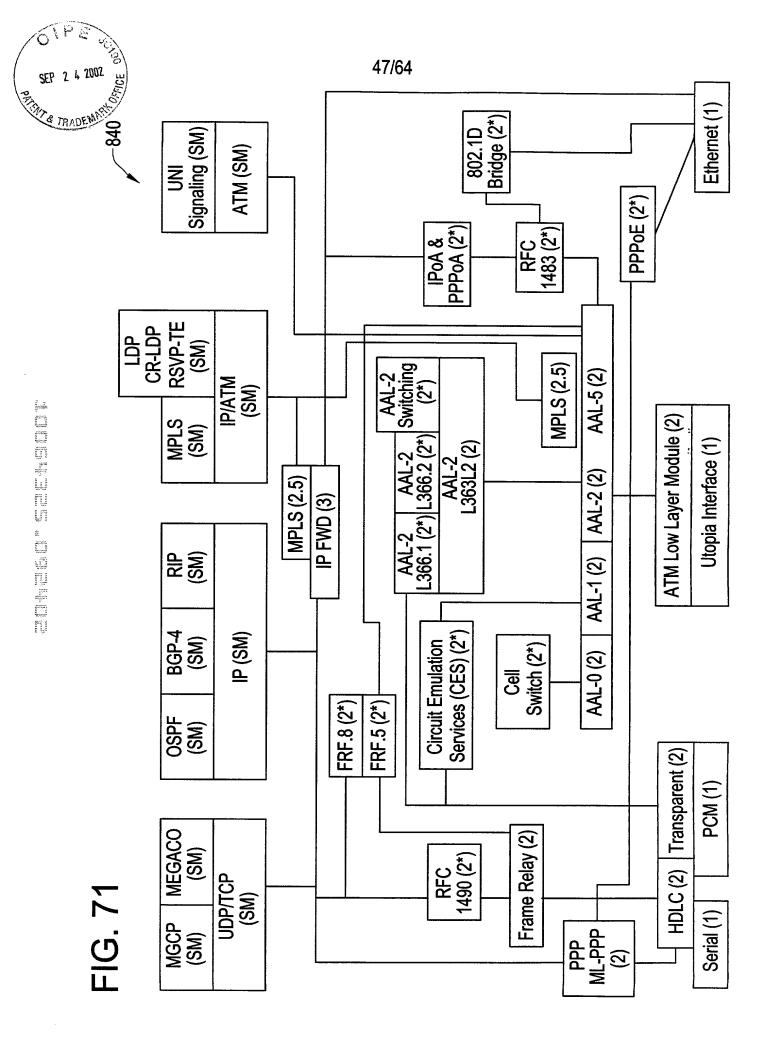


FIG. 69









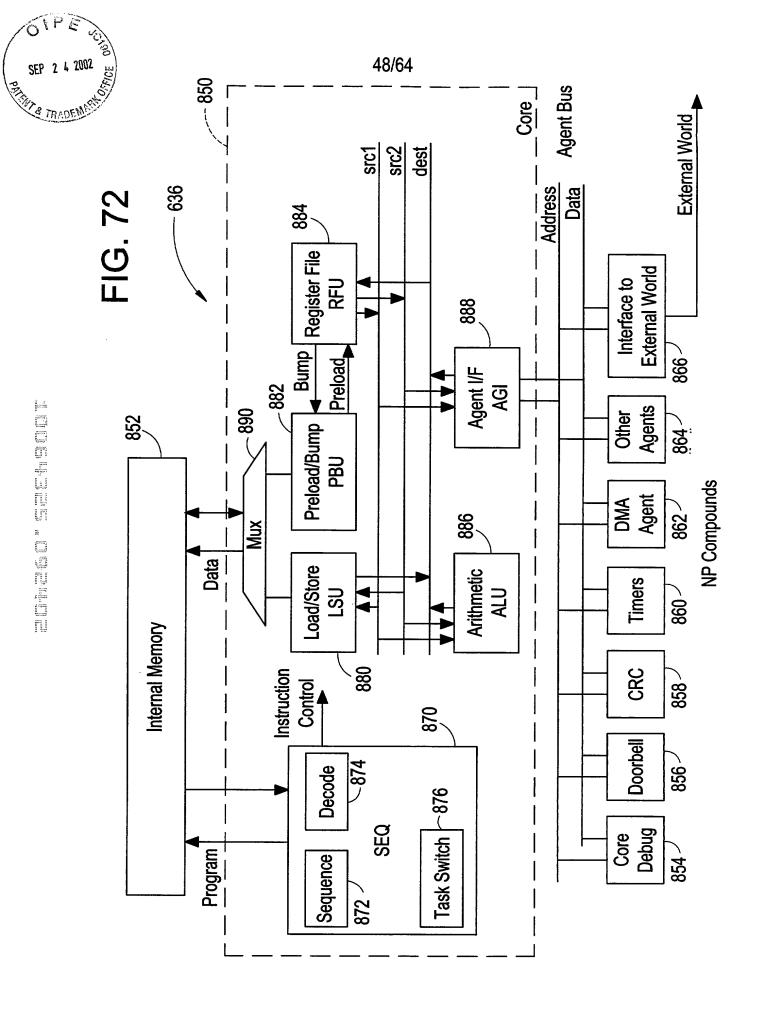




FIG. 74

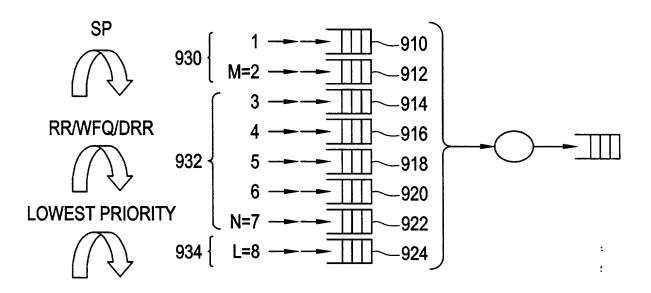
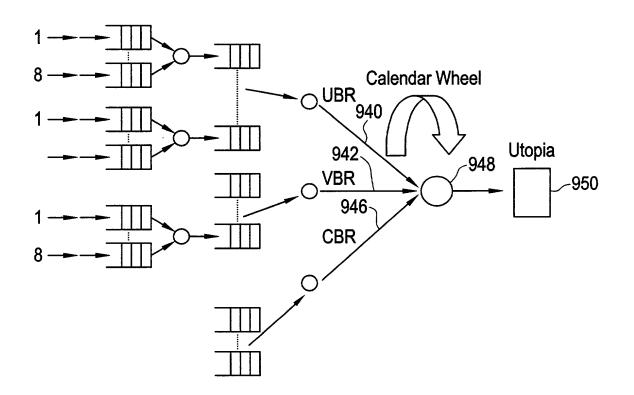
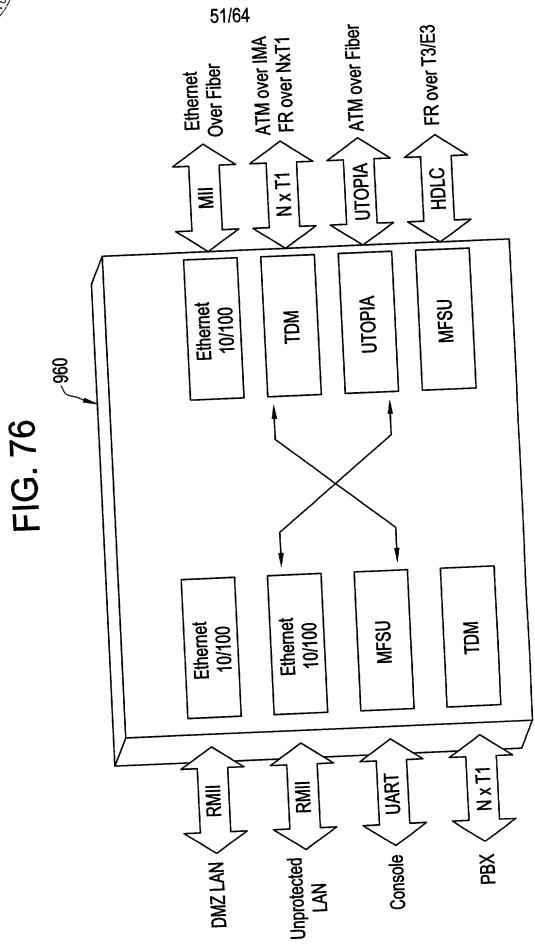
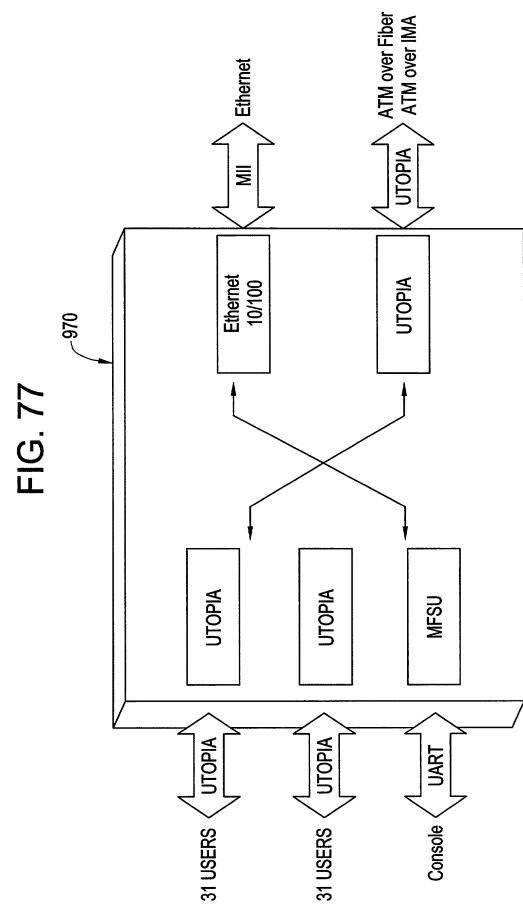


FIG. 75

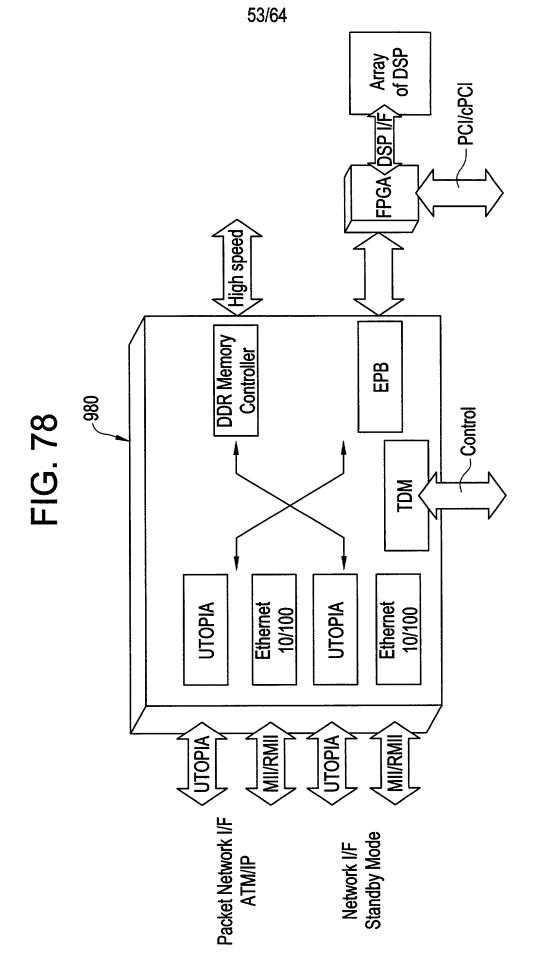




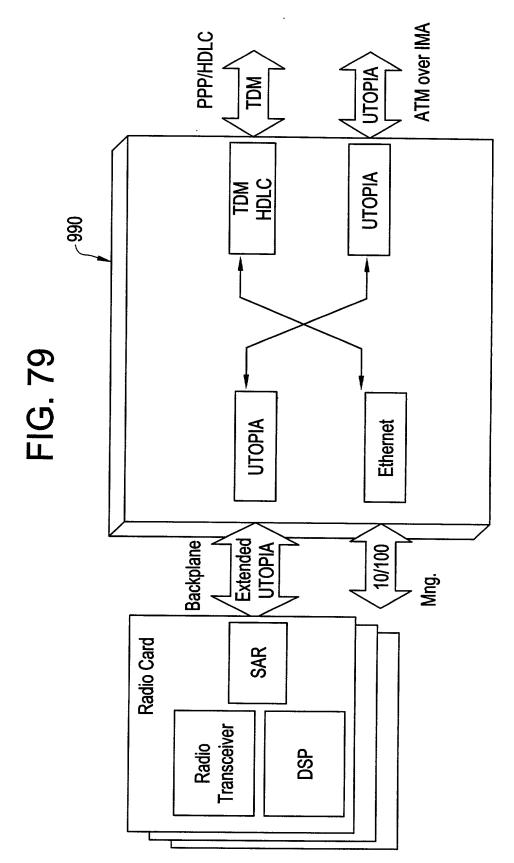




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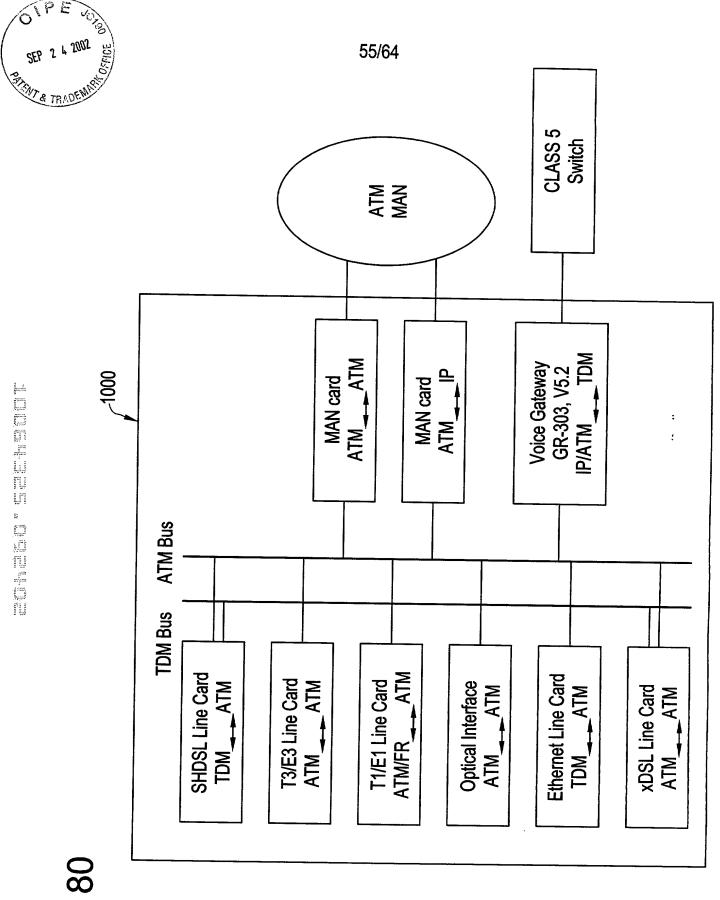
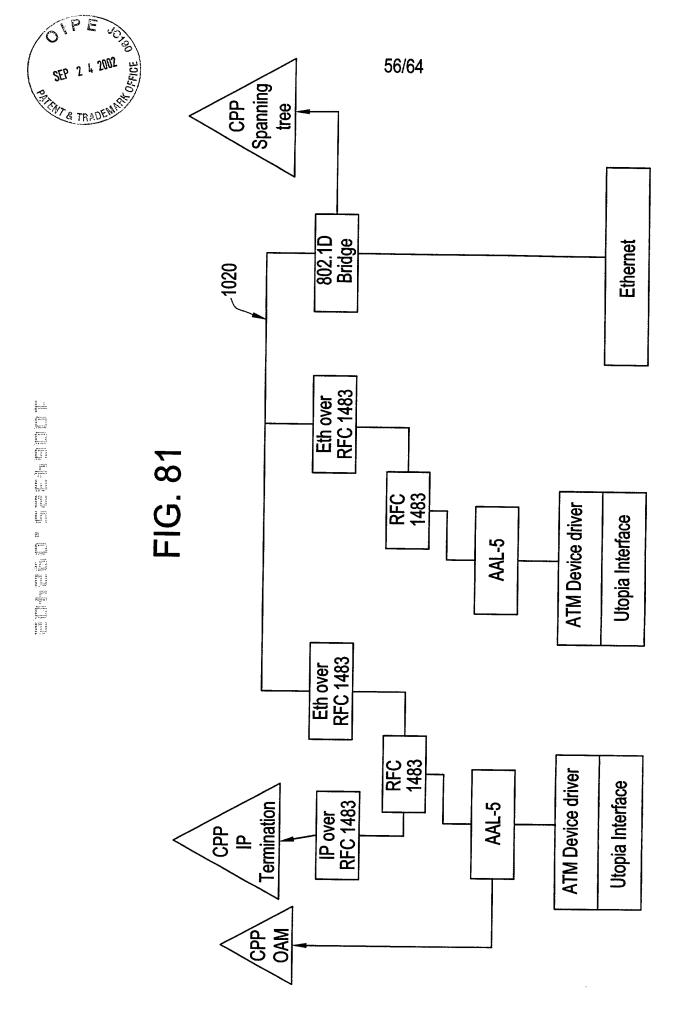
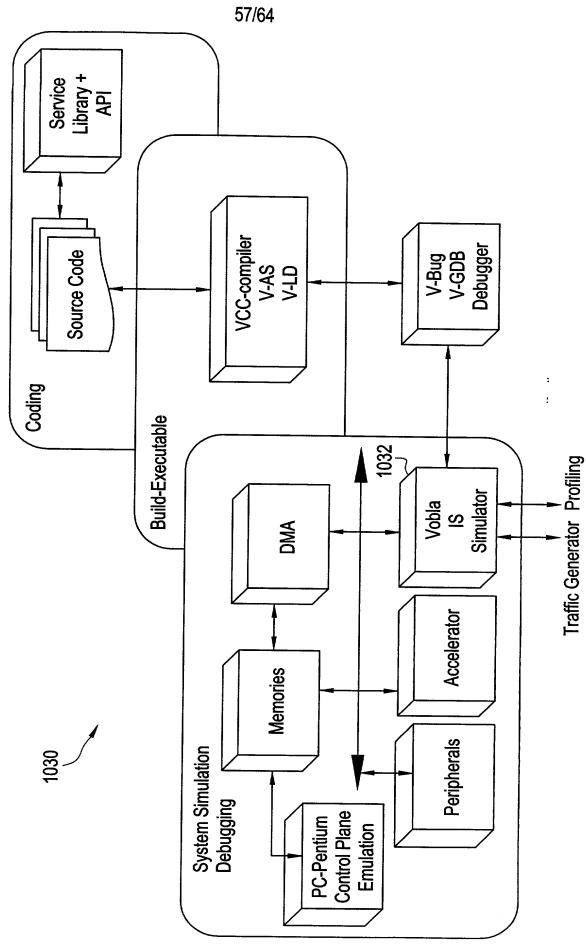


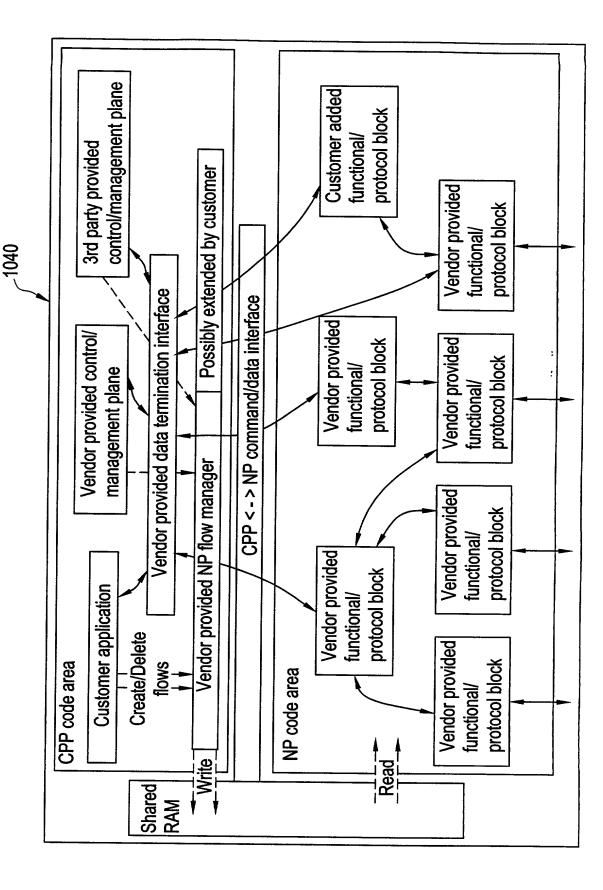
FIG. 80





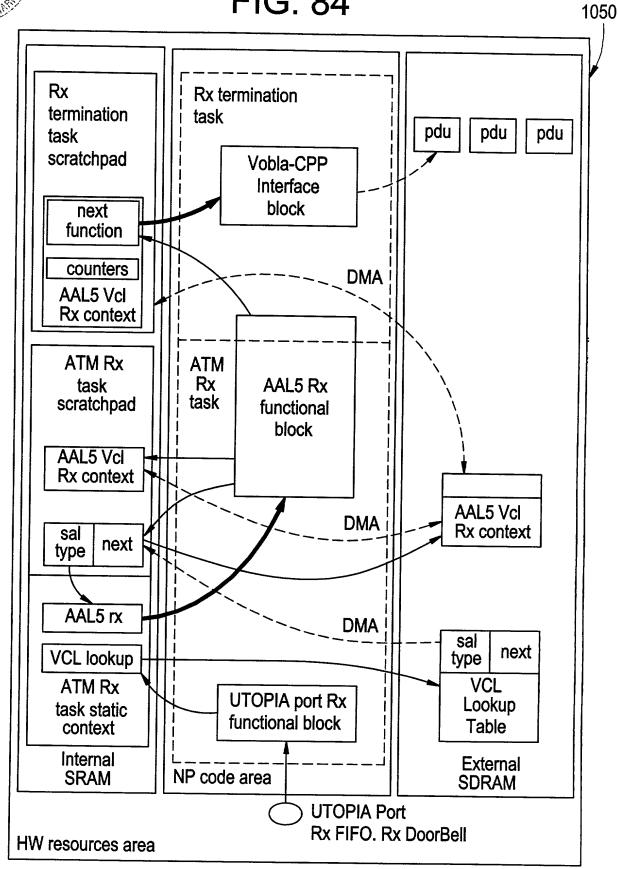


TRADEN!





SEP 2 L 2002 BY



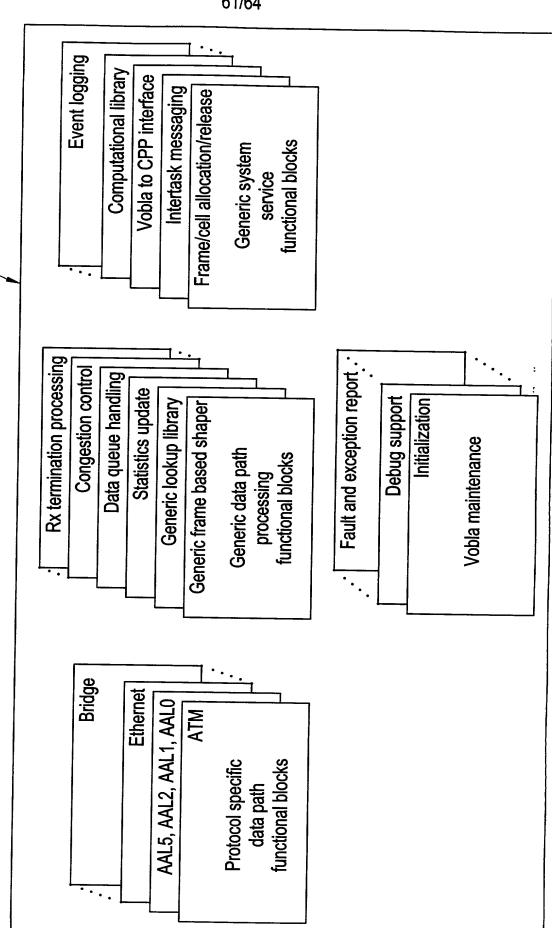
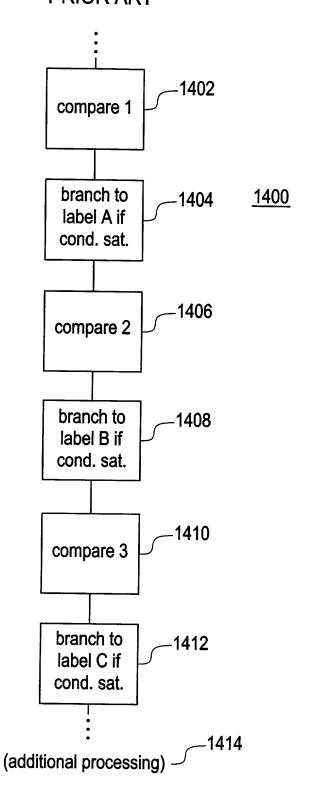




FIG. 87 PRIOR ART





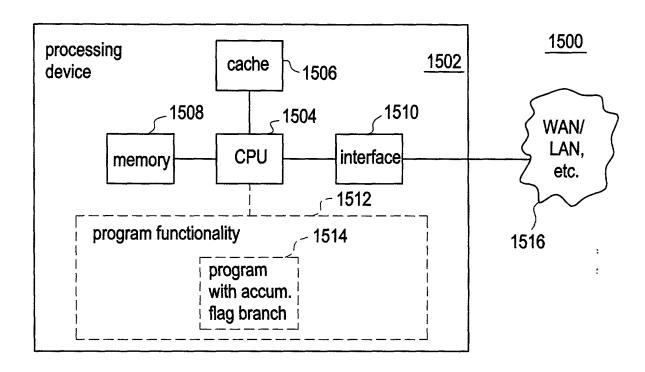


FIG. 89

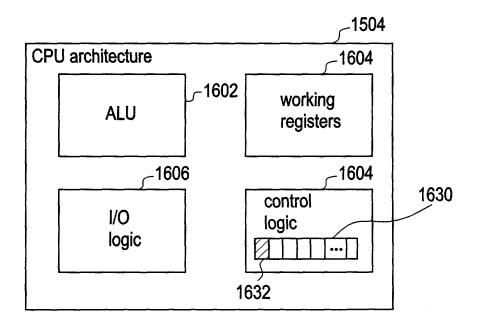




FIG. 90

